AT

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EXAMINER	
LEE, EUGENE	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AT

Office Action Summary	Application No.	Applicant(s)	
	10/663,051	MA ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the LOCOS process (claims 11, 25, and 39) and masked ion implant (claims 14, 28, and 40) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1 thru 19, and 21 thru 42 are objected to because of the following informalities: (1) in line 2 of claim 1, for example, the limitation "first conducting type" should be "first conductivity type" or "first dopant type"; and (2) in claim 6 (also claim 18), there is an unnecessary comma in line 2 in between the limitation "comprising" and "a common drain region." Appropriate correction and/or clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 18, 19, 21, 23, 25 thru 28, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams et al. 5,386,136. Williams discloses (see, for example, FIG. 9) a semiconductor device comprising a p epitaxial region (active region of a first conducting type) including a transistor structure, wherein the transistor structure comprises an N+ region (drain) 908, first source region, second source region, first and second channels, first and second gates, and a P-body (ring shaped region of the first conducting type). In column 8, lines 29-32, Williams discloses the P-body as being an annular structure (ring shaped).

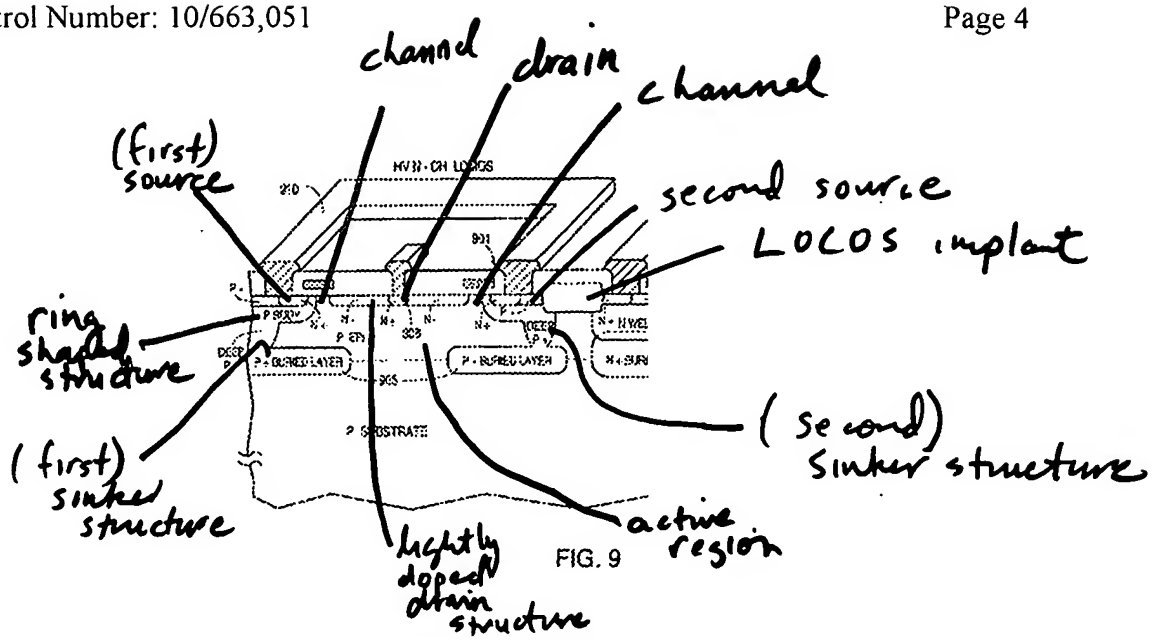

FIG. 9

Regarding claim 21, see, for example, FIG. 9 wherein Williams discloses an N- region (lightly doped drain region) next to the N+ region 908.

Regarding claim 25, see, for example, FIG. 9 wherein Williams discloses a LOCOS implant enclosing the semiconductor device.

Regarding claim 26, see, for example, FIG. 9 wherein Williams discloses a P substrate and P epitaxial layer.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 10, 11, 13 thru 16, 32, 38, 39, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki 6,258,640 B1 in view of Arai et al. 5,192,993. Miyazaki discloses (see, for example, FIG. 2K) a semiconductor device comprising a P-type well region

(active region of a first conducting type) 12, including a transistor structure comprising a drain region 22, source region 22S, channel, gate electrode (gate) 20, and guard ring 18. The guard ring overlaps the source region 22S and, substantially surrounds the transistor structure. Miyazaki does not disclose a stripe shaped drain region and a stripe shaped source region, wherein the drain and the source define a stripe shaped channel. However, Arai discloses (FIG. 2A) a semiconductor device comprising a transistor comprising a stripe shaped drain/source area 14, guard ring 18, and polysilicon connection layer (gate) 22. It would have been obvious to one of ordinary skill in the art at the time of invention to have a stripe shaped drain region and a stripe shaped source region, wherein the drain and the source define a stripe shaped channel in order to form a lateral transistor.

Regarding claims 10, and 38, Miyazaki in view of Arai does not disclose the ring being doped in the range of 10^{14}-10^{15}/cm^2. However, doping the ring in the range of 10^{14}-10^{15}/cm^2 is a result effective variable for the withstand voltage of a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the ring doped in the range of 10^{14}-10^{15}/cm^2 in order to establish the withstand voltage of the semiconductor device, and since it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 11, and 39, see, for example, FIG. 2K wherein Miyazaki discloses a device isolation insulating film (LOCOS process) 16.

Regarding claims 15, and 41, see, for example, FIG. 2E wherein Miyazaki discloses boron ions implanted to form the boron ions implanted layer 17, and the subsequent guard ring 18.

7. Claims 2 thru 4, 6, 7, 9, 12, 33 thru 35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki '640 B1 in view of Arai et al. '993 as applied to claims 1, 10, 11, 13-16, 32, 38, 39, 41, and 42 above, and further in view of Williams et al. 5,386,136. Miyazaki in view of Arai does not disclose the transistor structure further comprising a sinker structure of said first conducting type. However, Williams discloses (see, for example, FIG. 9) a transistor comprising a P+ buried layer (sinker structure) 905. In column 8, lines 26-27, Williams discloses the P+ buried layer as a field–shaping structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the transistor structure further comprising a sinker structure of said first conducting type in order to shape the electric field.

Regarding claims 4, 7, and 35, Miyazaki in view of Arai does not disclose the drain region comprising a lightly doped drain region. However, Williams discloses (see, for example, in FIG. 9) a N- layer (lightly doped drain region) next to a N-+ region (drain) 908. Lightly doped drain regions suppress leakage current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the drain region comprising a lightly doped drain region in order to suppress leakage current.

Regarding claims 6, and 34, Miyazaki in view of Arai does not discloses the transistor

structure being a two transistor structure comprising a common drain region, a first source region arranged on one side of the common drain region, a second source region arranged on the respective opposite side of the drain region, wherein the drain region and the source regions each define a channel, a first and second gate being arranged above said channels, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area. However, Williams discloses (see, for example, FIG. 9) discloses two transistors sharing a N+ regions (common drain region) 908, have a first source region and a second source region each defining a channel and first and second deep+ regions (first and second sinker structure). The two transistors provide a structure for a high voltage laterally diffused MOS transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have the transistor structure being a two transistor structure comprising a common drain region, a first source region arranged on one side of the common drain region, a second source region arranged on the respective opposite side of the drain region, wherein the drain region and the source regions each define a channel, a first and second gate being arranged above said channels, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area in order to form a high voltage laterally diffused MOS transistor.

Regarding claim 12, Miyazaki in view of Arai does not discloses the active area comprising a substrate and an epitaxial layer on top of said substrate. However, Williams discloses (see, for example, FIG. 9) a P substrate and a P epitaxial layer. The P substrate and P

epitaxial layer support the transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the active area comprising a substrate and an epitaxial layer on top of said substrate in order to adequately support the transistor.

8. Claims 5, 8, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki '640 B1 in view of Arai et al. '993 in view of Williams et al. '136 as applied to claims 2-4, 6, 7, 9, 12, 33, 34, 35, 37 above, and further in view of Leong 6,372,557 B1. Miyazaki in view of Arai in view of Williams does not disclose a metal layer on the backside of the semiconductor device. However, Leong discloses (see, for example, Fig 3L) a semiconductor device comprising a bottom side metalization layer (metal layer) 138. In column 4, lines 48-52, Leong discloses the bottom side metalization layer facilitates electrically grounding a substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a metal layer on the backside of the semiconductor device in order to facilitate electrically grounding the substrate of a semiconductor device.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki '640 B1 in view of Arai et al. '993 as applied to claims 1, 10, 11, 13-16, 32, 38, 39, 41, and 42 above, and further in view of Gajda et al. 6,780,714 B2. Miyazaki in view of Arai does not disclose the ring comprising at least one gap. However, Gajda discloses (see, for example, FIG. 5) a semiconductor device comprising a P diffusion ring region 15a separated by gaps 14x. In column 8, lines 54-56, Gajda discloses the gaps having no substantial effect on the ring operation of region 15a. Therefore, it would have been obvious to one of ordinary skill in the art at the

time of invention to have the ring comprising at least one gap since such a gap has no substantial effect on the operation of the semiconductor device and provides another way of efficiently forming the guard ring with less dopant.

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. '136 as applied to claims 18, 19, 21, 23, 25-28, and 30 above, and further in view of Leong 6,372,557 B1. Williams does not disclose a metal layer on the backside of the semiconductor device. However, Leong discloses (see, for example, Fig 3L) a semiconductor device comprising a bottom side metalization layer (metal layer) 138. In column 4, lines 48-52, Leong discloses the bottom side metalization layer facilitates electrically grounding a substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a metal layer on the backside of the semiconductor device in order to facilitate electrically grounding the substrate of a semiconductor device.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. 5,386,136. Williams discloses (see, for example, FIG. 9) a semiconductor device comprising a p epitaxial region (active region of a first conducting type) including a transistor structure, wherein the transistor structure comprises an N+ region (drain) 908, first source region, second source region, first and second channels, first and second gates, and a P-body (ring shaped region of the first conducting type). In column 8, lines 29-32, Williams discloses the P-body as being an annular structure (ring shaped). Williams does not disclose the ring being doped in the range of 10^{14}-10^{15}/cm^2. However, doping the ring in the range of 10^{14}-10^{15}/cm^2 is a result effective

variable for the withstand voltage of a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the ring doped in the range of 10^{14}-10^{15}/cm^2 in order to establish the withstand voltage of the semiconductor device, and since it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

12. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. '136 as applied to claim 24 above, and further in view of Miyazaki 6,258,640 B1. Williams does not disclose boron being used as a dopant. However, Miyazaki discloses (see, for example, FIG. 2E) boron ions implanted to form the implanted layer 17 and the subsequent guard ring 18. It would have been obvious to one of ordinary skill in the art at the time of invention to use boron as a dopant in order to form an adequate p-type guard ring.

13. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. '136 as applied to claims 18, 19, 21, 23, 25-28, and 30 above, and further in view of Gajda et al. 6,780,714 B2. Williams does not disclose the ring comprising at least one gap. However, Gajda discloses (see, for example, FIG. 5) a semiconductor device comprising a P diffusion ring region 15a separated by gaps 14x. In column 8, lines 54-56, Gajda discloses the gaps having no substantial effect on the ring operation of region 15a. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the ring comprising at least one

gap since such a gap has no substantial effect on the operation of the semiconductor device and provides another way of efficiently forming the guard ring with less dopant.

14. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki '640 B1 in view of Arai et al. '993 as applied to claims 1, 10, 11, 13-16, 32, 38, 39, 41, and 42 above, and further in view of Chang et al. 6,624,030 B2. Miyazaki in view of Arai does not disclose the ring being created by masked ion implant. However, Chang discloses (see, for example, FIGs. 6 and 7) a semiconductor device comprising a P diffusion ring 28 formed by a boron implant and photoresist (masked) 52. It would have been obvious to one of ordinary skill in the art at the time of invention to have the ring created by masked ion implant in order to form a ring adequately in a substrate.

Response to Arguments

15. Applicant's arguments with respect to claims 1-19, and 21-42 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the applicant's arguments towards the drawing objections, the figures do not show any features of a LOCOS or a mask. Since these features are stated specifically in the claims, they must also be shown in the drawings.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
February 14, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER